

## G320 BLOCK DIAGRAM

## HOW THE G320 WORKS:

The STEP and DIRECTION inputs to the top 8-bit up/down counter. The quadrature encoder is decoded into CLOCK and DIRECTION signals that input into the bottom 8 -bit up/down counter. There is a CLOCK pulse for every encoder edge, (X4 decoding).

The accumulated counts of each counter are input to an 8 -bit adder. The adder's sum of these inputs is applied to an 8 -bit D to A converter. The carry bit is discarded.

In normal operation, one counter increments while the other counter decrements. The initial offset between the counters is 80 H , set while the drive is in power-on reset. The incrementing counter's contents will be $80,81,82 \mathrm{H}$, etc. for every STEP pulse, while the decrementing counter's contents will be, 00, FF, FE, etc. for every encoder edge. The sum will stay at a constant 80 H at the adder's sum output if the carry bit is neglected.

The D to A scale is set such that 00 H is 0 VDC while FFH is 10 VDC . Therefore 80 H is 5VDC, indicating zero difference error. This node is available for measurement at the TEST POINT.

This is the POSITION ERROR node of the circuit. Every 40 mV above 5VDC is one motor increment of position ahead of "zero" error while every 40 mV below 5VDC is one increment of motor position behind the "zero" error location (10VDC/256 $=40 \mathrm{mV}$ ).

This voltage is split 3 ways and sent to the PID channels. One channel is proportionally amplified, gain set by the " P " co-efficient, (GAIN trimot). The next channel is differentiated, gain set by the "D" co-efficient, (DAMP trimpot). The final channel is integrated, gain set by a fixed "l" co-efficient. All three channels are then summed and input to the pulse-width modulator (PWM).

The PWM pulse-width modulates a 25 kHz frequency that then is sent in true and complimentary forms to the half-bridge drivers that control the power n-channel MOSFETs that drive the motor.

Motor current is sensed by the 0.025 Ohm current sense resistor. This current is compared against a reference set by the current LIMIT trimpot. If motor current reaches this reference, all four MOSFETs are shut off for the balance of the switching cycle, limiting motor current on a cycle-by-cycle basis. A second comparator has a reference set to 21 A, if motor current reaches this value, the comparator sets the FAULT latch, shutting down the drive.

A window comparator whose reference limits are set to about $+/-120$ increments of position error monitors the POSITION ERROR signal. This window comparator also sets the FAULT latch should the POSITION ERROR reach these limits.

The FAULT latch lights the FAULT LED when set and outputs a logical "0" on the ERR/RES terminal of the drive. This terminal also functions as a RESET input. If this terminal is forced to a logical "1", it starts a 5 second timer that clears the FAULT latch, if set, and re-enables the drive.

If this terminal is forced to a logical "0", it will immediately setting the drive into FAULT, shutting off the power MOSFETs and free-wheeling the motor.

## NOTES:

The power MOSFETs used are 100V, 27Amp rated TO-220 devices.
The drive behaves exactly like a step motor drive. The motor has holding torque up to the motor's stall torque or the current limit of the drive. There is no minimum speed; the motor will move in step increments equal to the encoder resolution. The motor will track the STEP pulse rate and move a distance equal to the steps sent.

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